REMARKS

Applicant has included a fee transmittal with this Preliminary Amendment authorizing the Commissioner to charge any appropriate fees to Deposit Account Number 50-0441.

The Westberg patent is related to a "video computer system" that allows legacy execution of older and newer developed programs. In Westberg, a microprocessor controls two video controllers and instructs a select circuit to produce the appropriate video output depending upon which video controller is compatible with the graphics programs stored in memory that is being run. That is, only one video controller will actually be used for any given software application. Thus, the Westberg patent teaches an opposite approach from the use of two video controllers to provide video output for the same software application. The Westberg system selects from one of two available video signals for display, and thus teaches away from any embodiment that uses or facilitates the use of two cooperating video controllers or two video output ports.

An inherent feature of Westberg is that it does not teach, inter alia, the use of a second video output port. As discussed at column 4, lines 35-44, the microprocessor accesses the graphics program stored in read only memory and determines whether the program was designed to be compatibly executed (i.e., processed) by a first video graphics controller or by a second video graphics controller. The microprocessor then correspondingly generates a signal to select the compatible graphics controller and instructs the select means to select the video output of the selected video graphics controller.

In contrast, in Claim 1 as amended, Applicant claims, inter alia, a second graphics device having an input and a first video component output to provide a first video output component signal; and a second video output port coupled to the first video component output of the second graphics device. This corresponds to an embodiment discussed at page 5, lines 19-21 of the Specification in which a first VGA (i.e., video graphics controller) will provide a video signal to a first video port, while a second VGA will provide a video signal to a second video port. As further discussed at page 4, lines 15-17, in a second embodiment, a first VGA renders an entire frame of video and provides it to an output port through a switch, and the next adjacent frame will be calculated by a separate VGA and provided to the output port through the switch. That is, in either embodiment, two separate video graphics controllers process portions of the same

input video stream, providing alternating frames to the same or different video output ports. Applicant is unable to find such teachings in Westberg. Moreover, there is no suggestion or motivation other than Applicant's own invention to use two video controllers to provide video output from a common source to two different ports. The Westberg reference further fails to teach, suggest, or require the use of two video controllers to provide video output from a common source to one port by, for example, alternating the output of frames between the two controllers as claimed. In fact, Westberg teaches away from the use of multiple cooperating video controllers, two video output ports, or any combination thereof, and teaches an opposite approach than that of the present invention. Accordingly, Claims 1 and 18 are believed to be allowable in light of Westberg.

Similarly, in Claim 19 as amended, Applicant claims, inter alia, generating a second signal at a second device, wherein the second signal is representative of a first video output component; and providing the second signal of the second device to a first output node. Applicant respectfully reasserts the relevant remarks with respect to Claim 1 above. Accordingly, Applicant believes Claims 19-22 to be allowable.

As to new Claim 29, Applicant claims, inter alia, wherein the first graphics device renders a frame of video and provides the rendered frame to the first video output port, and wherein the second graphics device renders an adjacent frame of video and provides the adjacent frame to the first video output port. Applicant respectfully reasserts the relevant remarks with respect to Claim 1 above. Applicant further notes that, as discussed, Westberg teaches the use of one of a plurality of video graphics controllers to process video depending upon which video controller is compatible with the graphics programs stored in memory that is being run. Such a device teaches away from the use of multiple cooperating video controllers processing alternating adjacent frames of a video signal (see Specification, page 5, lines 4-5). Accordingly, Applicant believes Claim 29 to be allowable.

Applicant has made certain amendments to the specification. These amendments were made only to correct minor typographical errors and grammatical informalities. In addition, none of the amendments to the specification were made to distinguish any claim of the present application over the prior art or for any other purposes related to patentability. Further,

Applicant submits that none of these amendments introduce any new matter into the specification.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "Version with markings to show changes made."

Applicant respectfully requests that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

By: ______________________
Christopher J. Reckamp
Registration No. 34,414

Date: October 17, 2001

VEDDER, PRICE, KAUFMAN &
KAMMHOLZ
222 N. LaSalle Street
Chicago, IL 60601
(312) 609-7500
FAX: (312) 609-5005

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

Paragraph of Page 3 beginning at line 9 has been amended as follows:

Yet another problem associated with the prior embodiments is that each of the graphics devices has to calculate the shape of each and every object on the frame. Each device must calculate each object's shape in order to determine whether or not the object, or a portion of the object, must be further processed by the graphics engine associated with the graphics device. An associated problem[,] is that when an object [is] straddles the demarcation line between an area that the first graphics device is to process and an area that the second graphics device is to process, it is necessary for both devices to process the object. For example, when a portion of an object is in the top half of the screen, and a portion on the bottom half of the screen, calculations associated with the object are calculated by both graphic devices.

Paragraph of page 3 beginning at line 19 has been amended as follows:

Yet another problem with the known implementations of multiple graphic devices is the need to carefully match the digital-to-analog converters (DACs) associated with each VGA[s]. The DACs of each VGA provide a plurality of voltages, one for each video component, such as the red/green/blue components. If the DACs are not carefully matched, it is possible for colors viewed on a display device to have slightly different shades of color because of the lack of calibration between the devices' DACs.

Paragraph of page 8 beginning at line 8 has been amended as follows:

The Comparator 220 provides an output signal labeled COMPARE SIGNAL. The COMPARE SIGNAL will indicate when a match occurs between the voltage of the color component signal G and the VREF signal. In general, the COMPARE SIGNAL will toggle from an inactive state indicating the signals do not match to an active state indicating that the signals have matched. It will be understood by one of ordinary skill in the art that if the Comparator 220 were to comprise a simple differential amplifier, the COMPARE SIGNAL would maintain the active state indicating a match, even when the green signal attains a voltage level significantly

higher than the VREF signal. In other words, in the embodiment illustrated, the toggling of the signal COMPARE SIGNAL from one state to another indicates a match has occurred. The signal labeled ADJUST [SIGNAL] CONTROL is received by the Adjust Signal Generator 230. The Adjust Signal Generator 230, in response to a signal from Control 130 received as part of the ADJUST SIGNAL CONTROL, provides a signal labeled ADJUST SIGNAL. In a specific embodiment, the ADJUST SIGNAL GENERATOR 230 is a variable reference source. The ADJUST SIGNAL provides a value for calibrating the DAC values of at least one of the VGAs.

Paragraph of page 9 beginning at line 4 has been amended as follows:

In operation, at least a portion of the VGA1 CONTROL signal is received by the first video controller 310. As illustrated, the VGA1 CONTROL signal comprises N signals that are received by the first video-out controller. In addition, the VGA1 Control signals are received by the Synchronize Device 350. It should be noted that M and N may be the same value. Likewise, the signal VGA2 CONTROL is received by the second video-out controller labeled VIDEO OUT2 CONTROL 320, and the Synchronize Device 350. Information transmitted over the LOCAL BUS is also received by the video-out controllers 310 and 320. It should be noted that information [ever] <u>over</u> the Local Bus will generally be received by the controller 130 at a single port, whereby the data can be provided to one or both of the two video-out controllers as appropriate. [(ED IS THIS ACCURATE FOR THE LOCAL BUS)]

Paragraph of page 10 beginning at line 21 has been amended as follows:

At step 420, the first signal is provided to a first node. With reference to Figure 1, the node is one of the plurality of nodes carrying the RGB1 signal. It should be noted that in the embodiment illustrated, that the RGB1 signal is provided to a bus comprising three nodes, one for each color component. Likewise, the RGB[L]2 signal is provided to a bus comprising a node for each color component.

Paragraph of page 10 beginning at line 26 has been amended as follows:

Next, at step 430, a value associated with the first signal and the first output node is determined. With reference to Figures 1 and 2, the signal[s] RGB OUT1 is provided to the Multiplexor 210 of Figure 2. One of the RGB signals is chosen at the analog Multiplexor 210 of

Figure 2, and provided to the Comparator 220. In the specific implementation illustrated, the values of the color components associated with the RGB OUT1 signal are voltage values. In other implementations, values other than voltages, i.e. current values, can be provided to Video-Out Adjust 160 of Figure 1. A specific implementation for determining the value during step 430 is to have the first VGA 110 change the value of the monitored color component (green in this example) until the value received at Comparator 220 matches VREF. This is accomplished by having the Controller 130 indicate to the VGA 110 to change the digital value of the DAC. By changing the digital DAC value the value received at the Comparator 220 of Figure 2 will also change. By monitoring the compare signal associated with the Comparator 220, the digital DAC value at which the first signal in step 420 matches VREF can be determined.

Paragraph of page 11 beginning at line 12 has been amended as follows:

At step 440, a second signal is generated at a second graphics device. With reference to Figure 1, the signal being generated would be the RGB2 signals by VGA 120. When the RGB1 signal and the RGB2 signals are to provide[d] alternating frames of video to Video Port1, it is necessary to compensate the values of the two VGAs 110 and 120 so that their RGB output values are approximately the same for given digital DAC value. If the output voltages of RGB1 and RGB2 are not the same for a given DAC value, variations in color will be detectable when switching [between] occurs between VGAs 110 and 120. Therefore, at step 440, the color component signal that is to be calibrated to the first signal will be generated using the value determined in step 430.

Paragraph of page 14 beginning at line 3 has been amended as follows:

Figure 5 illustrates another method in accordance with the present invention. At step 510, a first signal is generated representing a first color component of a first frame, and a second signal is generated representative of the first color component for a third frame of video [of video]. The first and second signals are both generated on a first VGA. With reference to Figure 1, the first and second video signals can be generated by the first VGA 110.

Paragraph of page 14 beginning at line 20 has been amended as follows:

In accordance with the present invention, the steps 510 through 550 are advantageous in that the workload distribution is approximately even because each VGA processes an entire frame of video, each frame of data is sent only one time to one VGA, each shape of a frame is calculated only once by one VGA, and there is no straddle data to burden down both processors. In addition, the voltage equalization as described within the method of Figure 2 also provides the advantage of allowing for even color reproduction regardless of the VGA driving an output port.

Paragraph of page 14 beginning at line 27 has been amended as follows:

[ ]It should be further understood that the specific steps of Figures 4 and 5 can actually be implemented in hardware and/or in software. For example, the various steps of generating signals can be performed by a hardware engine of the graphics controllers 110 and 120, or the steps can be performed in firmware, such as in microcode, executed on the processing engine associated with the controllers 110 and 120, or it may even be performed fully in software on a central processing unit. In general, a system for rending video may include a processing module and memory. The processing module may be a single processing device or a plurality of processing devices. Such a processing device may be a microprocessor, microcontroller, digital signal processor, microcomputer, portion of the central processing unit, state machine, logic circuitry, and/or any device that manipulates signals (e.g., analog or digital) based on operational instructions. The memory may be a single memory device or a plurality of memory devices. Such a memory device may be a read-only memory, random access memory, floppy disk memory, magnetic tape memory, erasable memory, portion of system memory, and/or any device that stores operational instructions in a digital format. Note that when the processing module implements one or more of its functions via a state machine or logic circuitry, the memory storing the corresponding operational instructions is embedded within the circuitry comprising the state machine and/or logic circuitry.

Claims:

1. (Once Amended) A video driver system comprising:

a first graphics device having an input and a first video component output to provide a first video output component signal;

a second graphics device having an input and a first video [output] component output to provide a first video output component signal;

a first video output port [having a first node] coupled to the first video component output of the first graphics device and the first video component output of the second graphics device; and

a second video output port [having a first node] coupled to the first video component output of the second graphics device.

29. (New Claim) A video driver system comprising:

a first graphics device having an input and a first video component output to provide a first video output component signal;

a second graphics device having an input and a first video component output to provide a first video output component signal;

a first video output port coupled to the first video component output of the first graphics device and the first video component output of the second graphics device; and

a second video output port coupled to the first video component output of the second graphics device;

wherein the first graphics device renders a frame of video and provides the rendered frame to the first video output port, and

wherein the second graphics device renders an adjacent frame of video and provides the adjacent frame to the first video output port.